FELIX - A Generic Platform for AI/ML in NPP Experiments

Eric Buschmann, Hucheng Chen, Mauricio Feo, Akshay Malige, Shaochun Tang, **Hao Xu**

haoxu@bnl.gov

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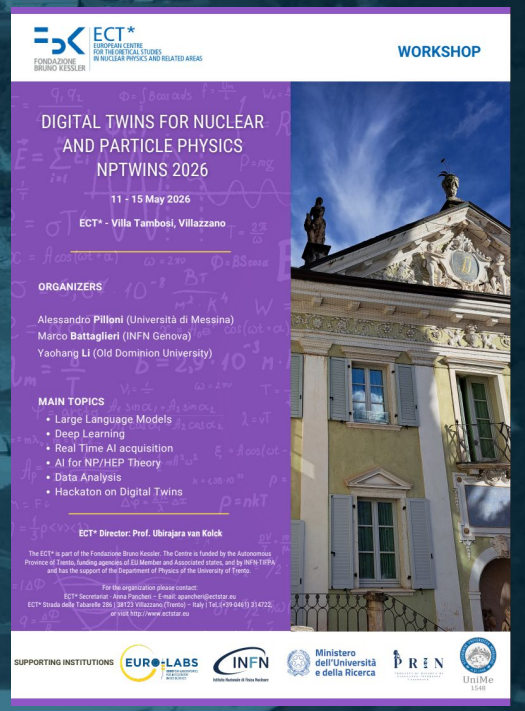
ECT* - Villa Tambosi, Villazzano



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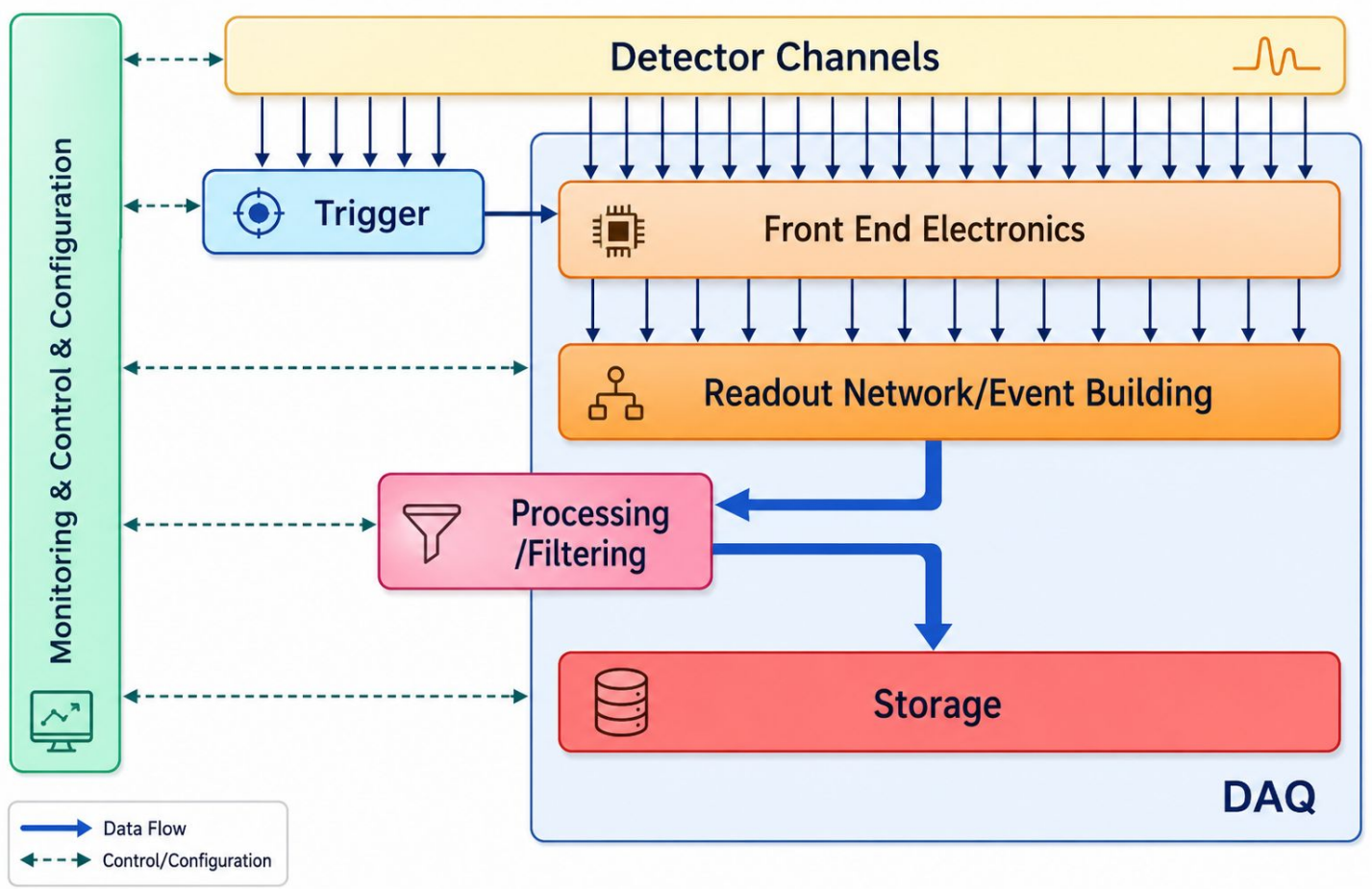
Outline

- Introduction to FELIX
- FELIX Hardware Development
- ATLAS EF Tracking on FELIX
- Summary

Real-time DAQ for NPP Experiment

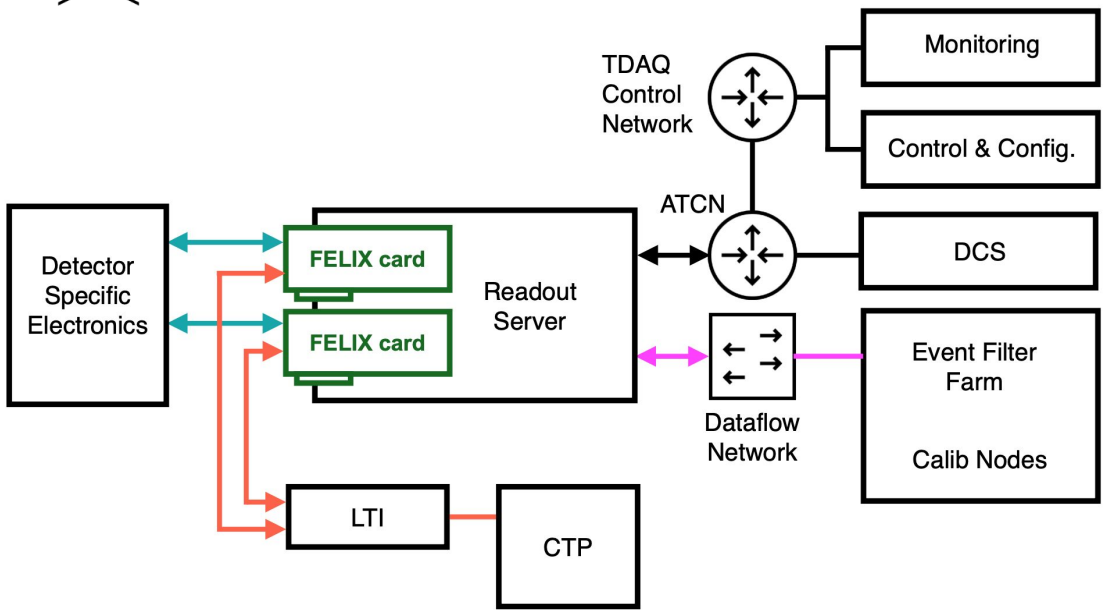


- Triggered readout
  - ATLAS
  - CMS
  - ALICE
- Streaming readout
  - LHCb (Run-3)
  - ePIC
  - CBM
- Hybrid readout
  - sPHENIX
  - ProtoDUNE-SP
  - SBND
  - DUNE

Block diagram of typical real-time data acquisition system

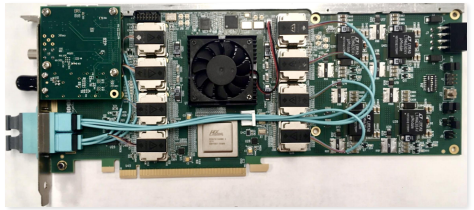
FELIX- Front-End LInk eXchange

- FELIX is a generic detector readout concept, proposed by ATLAS Collaboration a decade ago, between front-end serial links and a commodity network
  - https://atlas-project-felix.web.cern.ch/atlas-project-felix
  - Open-source firmware and software
  - Collaboration of different institutes
    - ANL, BNL, Bologna, CERN, IFIN-HH Bucharest, Nikhef, RU, RHUL, UC Irvine, Weizmann and Wuppertal
- Applications in HEP and NP experiments
  - ATLAS Phase-I Upgrade, ProtoDUNE-I and NA62
  - NSLS-II & ANL Light Source, sPHENIX at RHIC, SoLID at JLab, and FAIR CBM at GSI, Fermilab Test Beam
- Prospective Applications: ATLAS Phase-II Upgrade, EPIC@EIC, R&D of nEXO/DarkSide, ALICE and LHCb@HL-LHC



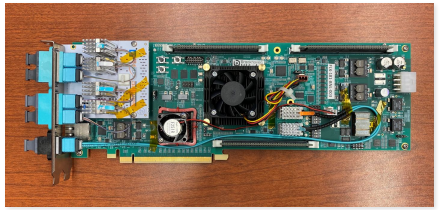
Block diagram of readout system of ATLAS for HL-LHC

FELIX Hardware Development @BNL

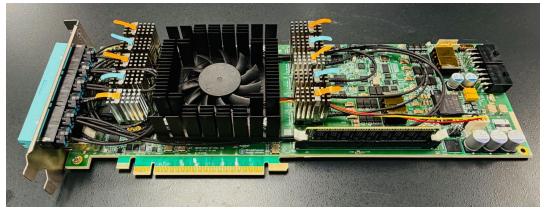


FLX-712
2018

PCIe Gen3 x16
48 x 10 Gb/s

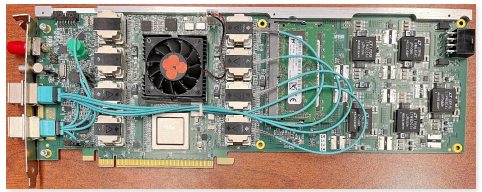


FLX-181
2020-21
PCIe Gen4 x16
FMC+ 16x 25 Gb/s + 12x 16 Gb/s
DDR4 · PetaLinux



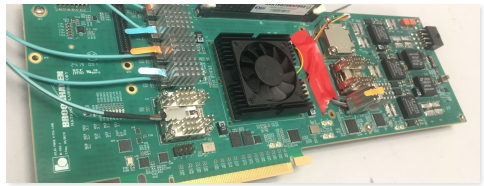
FLX-155
2024-2026
PCIe Gen4 x16/ Gen5 x8x8
(48+4) x 10/25 Gb/s
DDR4 · PetaLinux

FLX-711
2017



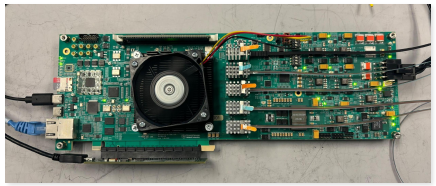
PCIe Gen3 x16
48 x 10 Gb/s · DDR3

FLX Demo for Ph-2
2019



PCIe Gen3 x16
25 Gb/s with various
optical modules

FLX-182
2022–23



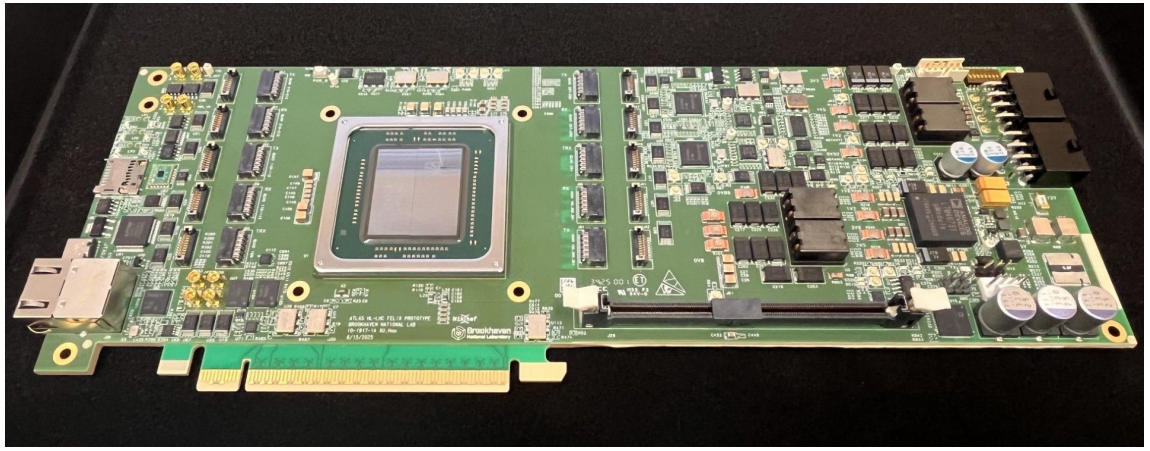
PCIe Gen4 x16
28x 10/25 Gb/s
DDR4 · PetaLinux

Long-term support for ATLAS Run 4 and beyond (2040+)

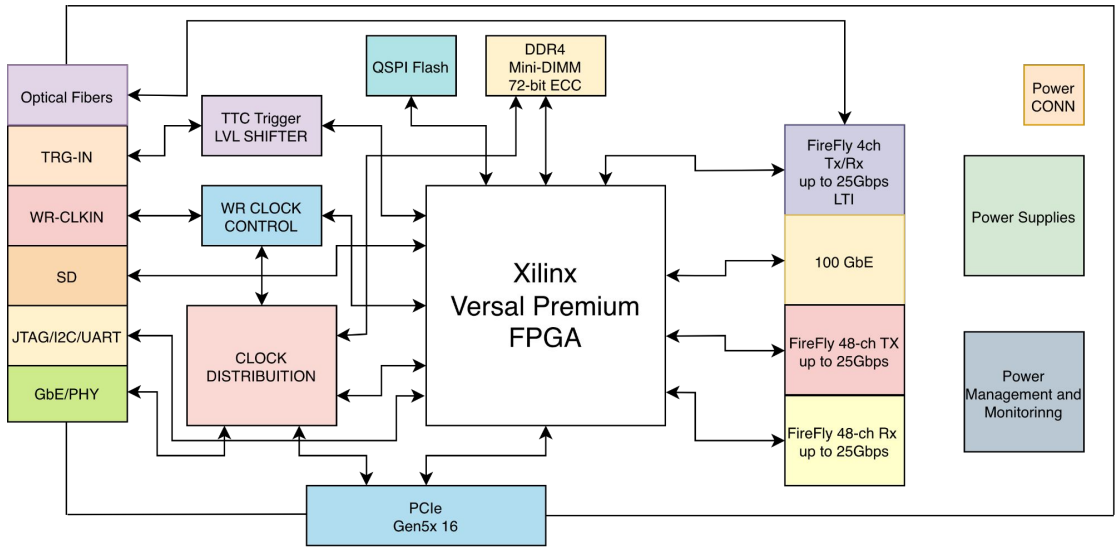
Brookhaven National Laboratory

FLX-155 Main Features

- AMD/Xilinx Versal Premium FPGA: XCVP1552-2MSEVSVA3340
- PCIe Gen4 x16/Gen5 x8x8
  - PCIe Gen5 x8x8 two endpoints implemented and tested. Each endpoint produced throughput of ~29.5 GB/s
  - ~98% of theoretical bandwidth
- 56 FireFly optical links
  - Compatible with various options
  - Default configuration
    - 48 data links up to 25 Gb/s
    - 4 links for LTI
    - 4 links for 100GbE
- Clock distribution
- White Rabbit
- Electrical IOs
- 1 DDR4 Mini-UDIMM
- USB-JTAG/USB-UART
- SD3.0/QSPI
- GbE



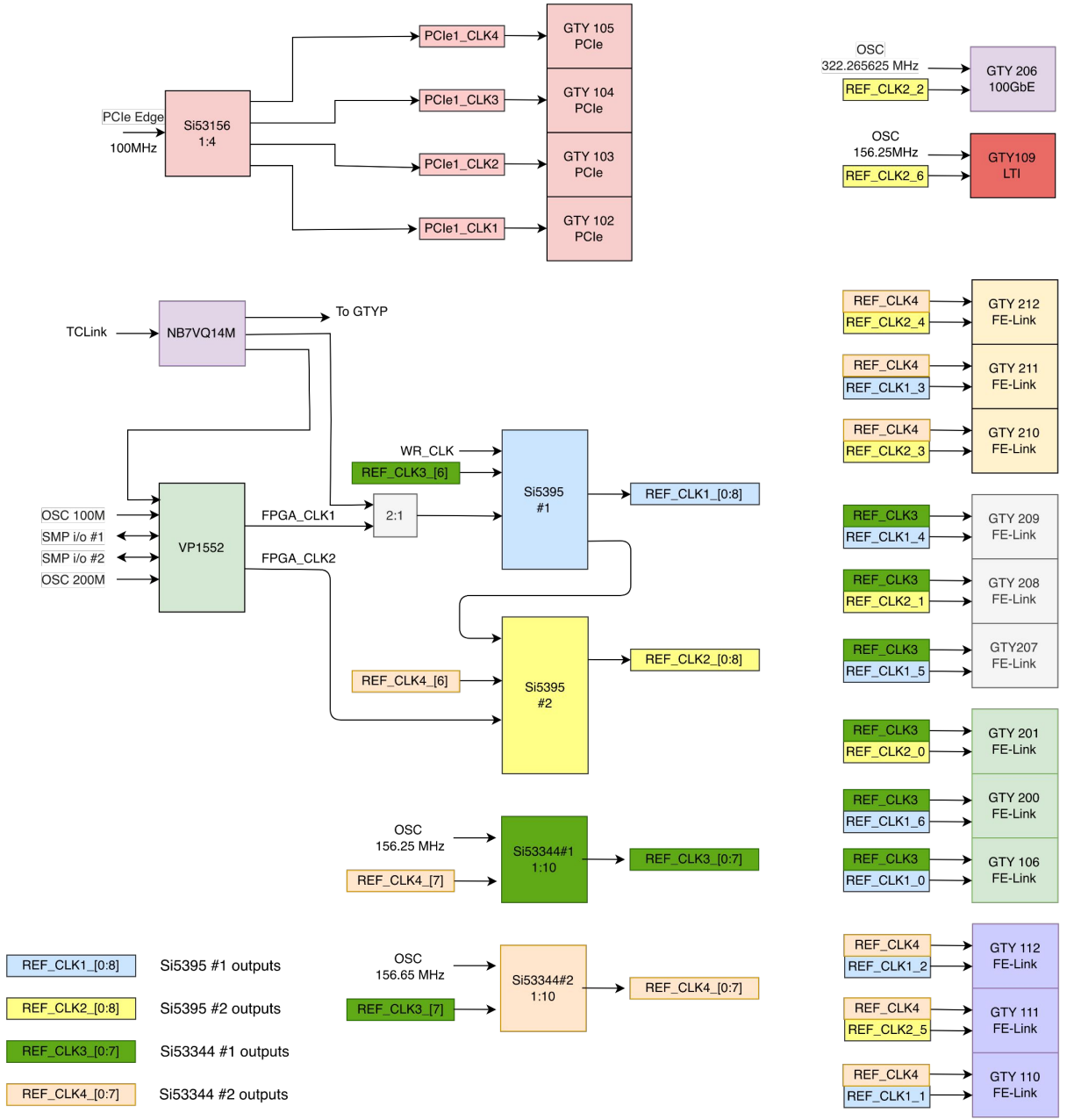
Picture of assembled FLX-155



Block diagram of FLX-155

Clock Distribution

- Si5395 jitter attenuators are used to clean the recovered clock from the LTI link and distribute it to the GTYP reference clocks
- Each GTYP data quad receives
  - One reference clock from a Si5395 output
  - A second reference clock from a Si53344 fanout buffer
- The LTI link uses
  - One reference clock from the Si5395, and
  - A secondary reference clock from an on-board oscillator
- 156.25 MHz oscillators are used as the primary on-board clock source to simplify the design
- The RX recovered clock phase from Versal GTYP transceiver is deterministic within tens of ps



Block diagram of clock distribution

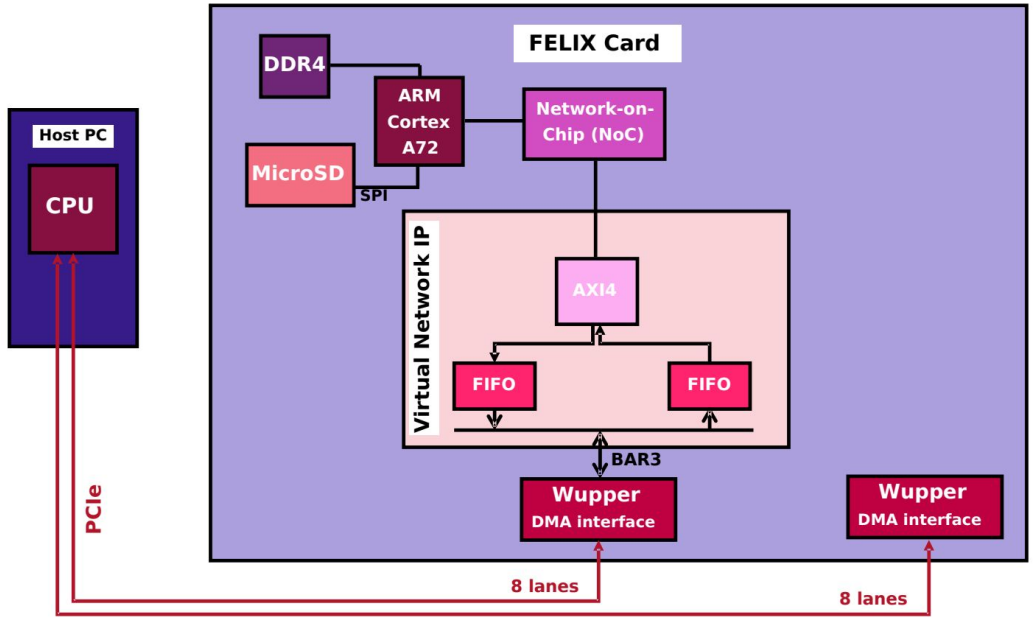
PetaLinux

- Arm cores in Versal Prime/Premium FPGA
  - Dual-core Arm Cortex-A72 Application Processor
    - Up to 1.7 GHz for 2X single-threaded performance
  - Dual-core Arm Cortex-R5 Real Processor
    - Up to 750 MHz for 1.4X greater performance
- The PetaLinux Tools offers everything necessary to customize, build and deploy Embedded Linux solutions on AMD processing systems
- PetaLinux can run successfully on Versal FPGA
  - Boot loader
  - CPU-optimized kernel
  - Linux applications & libraries
  - C & C++ application development
  - Integrated web server for easy remote management of network and firmware configurations



FPGA Boot

- Multiple boot modes are supported and verified on all boards
  - JTAG/SD/QSPI
- Remote firmware update
  - Golden image in QSPI
  - Boot images update and FPGA reconfiguration with FlxNet through PCIe
    - FlxNet is an internal network to the server, Linux drivers on the Versal ARM as well as the host enable flxnet as a regular network device

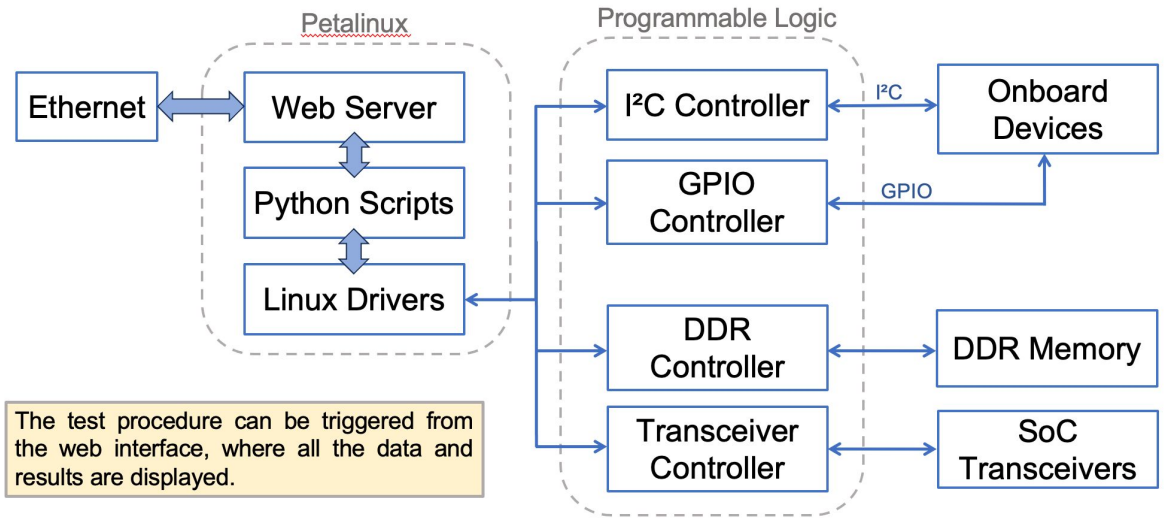


Block diagram of FlxNet: a virtual Ethernet connection over PCIe

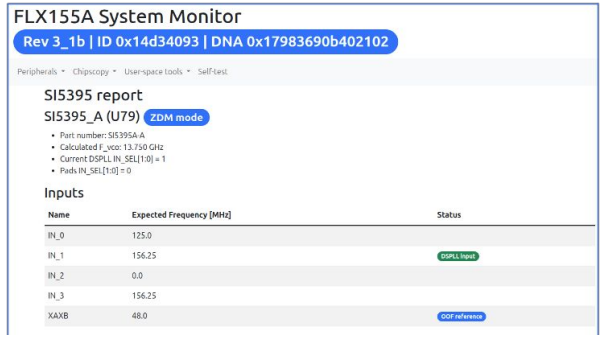
System Monitoring and Self-test

BIST: A Built-In Self-Test package with firmware and software for FELIX card validation

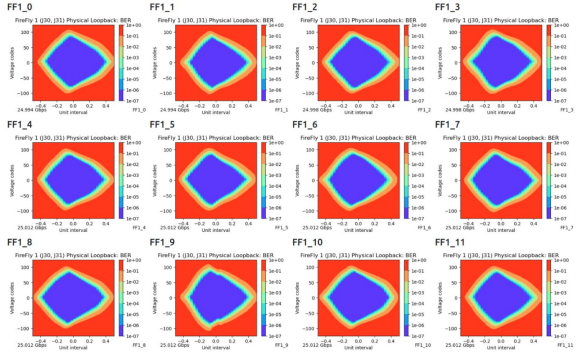
- Firmware and Software loaded from SD card
- Web page accessible through Ethernet over RJ45 connector or PCIe
- Web application
  - I²C, GPIO, and AXI drivers are the software interface to the gateware
  - Device-specific drivers control most devices (through I²C & GPIO)
  - SoC transceiver is controlled through the PS AXI bus. It is capable of running BER tests and generating Eye Diagrams during runtime
  - Python libraries provide the Web Application and functions to access board devices



Connectivity overview of BIST

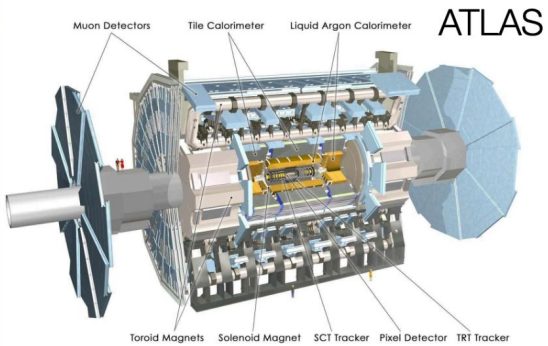


Web page of FLX155 BIST

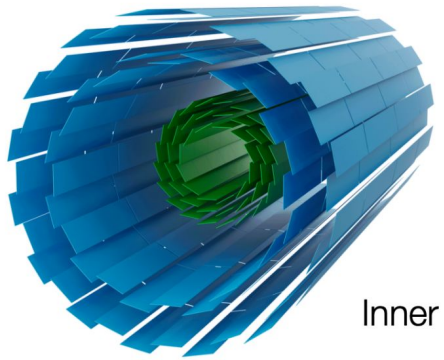


Eyescan results in BIST

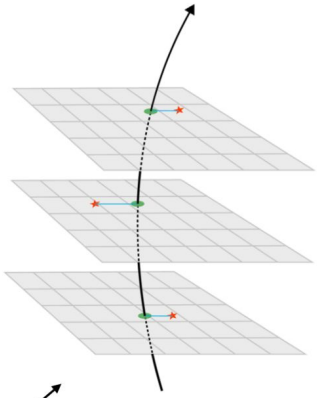
ATLAS Event Filter Tracking



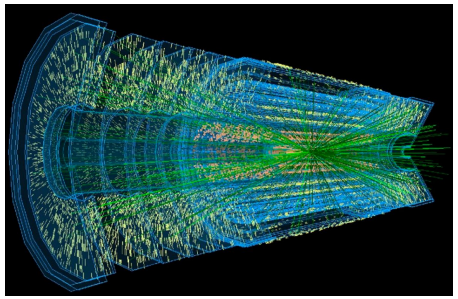
ATLAS detector

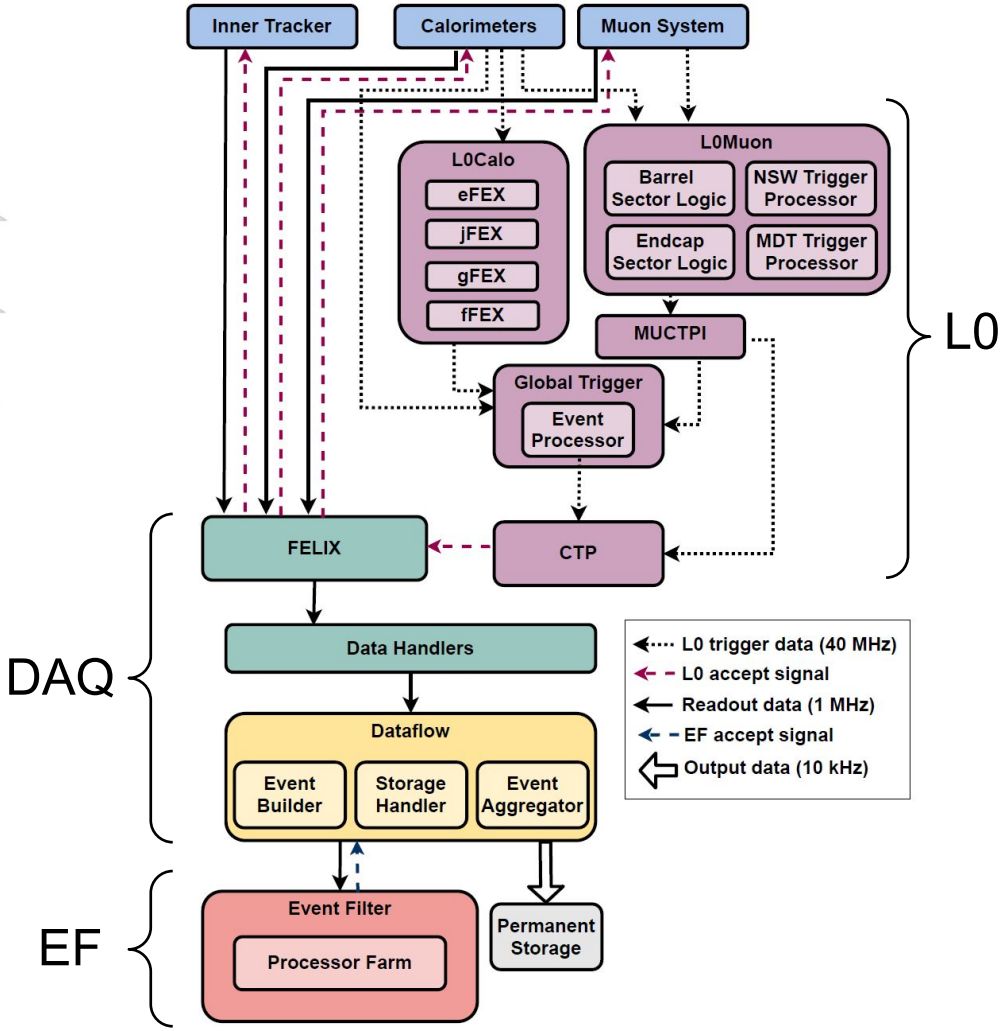


Inner tracker



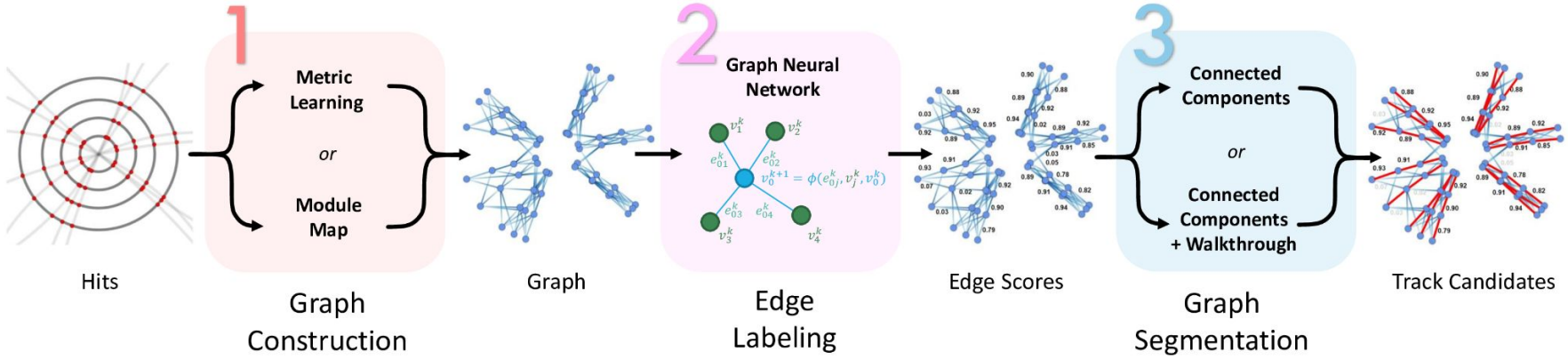
Reconstructing charged particles



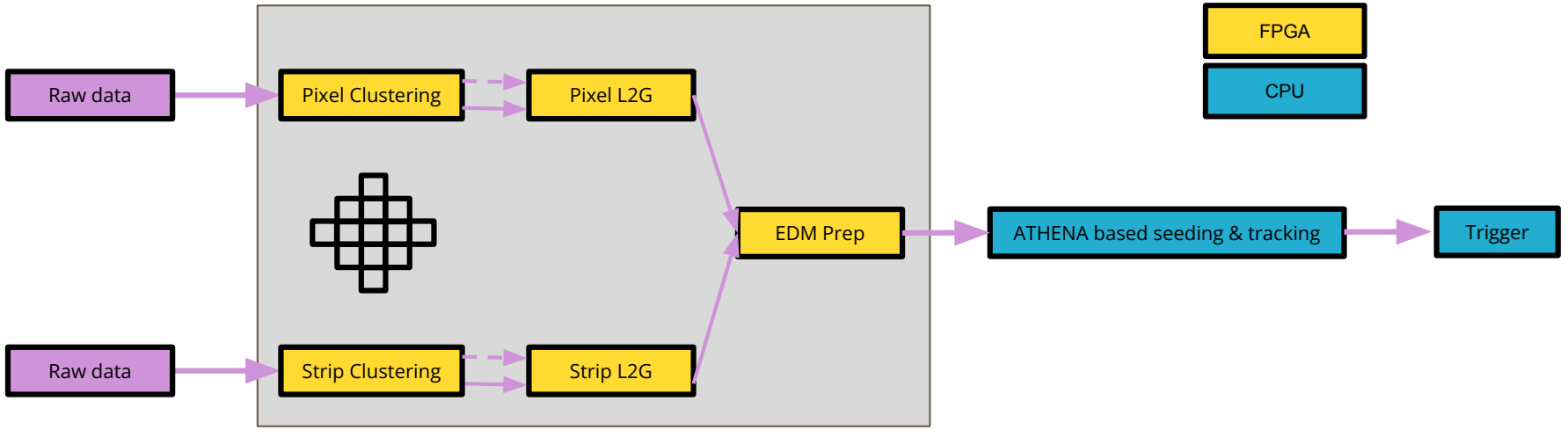


ATLAS TDAQ system

ATLAS EF Tracking Using GNN



Schematic overview of the GNN-based track finding pipeline

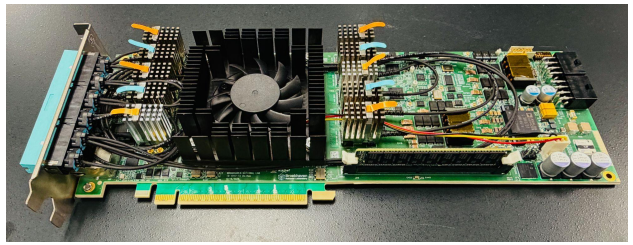


FPGA kernels - Clustering + global coordinate transformation + preparing output for xAOD EDM output

Alveo and FELIX

- Alveo U55, U250, or U280 are used in many HEP experiments
  - ATLAS EF tracking · LHCb ETX4-VELO · CMS · DUNE · CBM





Metric	Alveo U250	FELIX-155 (VP1552)	Edge
PCIe bandwidth	Gen3 x16 ~ 15.8 GB/s	2x Gen5 x8 ~ 63 GB/s	4x faster
Optical I/O	2x QSFP28 200 Gb/s	56x FireFly 1.4 Tb/s	7x more
Process node	16 nm	7 nm	Newer
Typical max clock	~300 MHz	~400 MHz	~33% higher
Typical power	110 W (max 225 W)	~80 W (board only)	~30% less
DSP engines	DSP58 (integer)	DSP58E2 (fp32+bf16)	Native float
AMD support	EOL approaching	~20-year lifespan	Long runway

EF Tracking on Alveo and FELIX

- ATLAS EF tracking F100 streaming pipeline has been implemented on Alveo and FLX-155
  - A large HLS design combining neural network inference (multiple NN models) with pixel and strip clustering, narrow-phase tracking, and EDM conversion
  - FLX-155 has less utilization, faster clock frequency and less power consumption

Metric		Alveo U250	FLX-155
Utilization (%)	DRAM	32	24
	DSP	3	3
	FF	11	4
	LUT	66	10
	LUTRAM	44	3
Kernel clock		250MHz	370MHz
Power Consumption		28.76W	22.32W
compile time		Long, struggles	~ 1 hour

https://github.com/AkshayMalige/felix-xpfm-project.git

Summary

- FELIX: a generic detector readout platform with open-source firmware/software and long-term support
- A powerful, flexible platform for AI/ML applications in NPP experiments
- ATLAS EF tracking on FELIX demonstrates these capabilities

Thanks!

FELIX Development Schedule

- March 2026: Production of five FLX-155 cards for ATLAS and ePIC integration tests
- April 22, 2026: ATLAS Final Design Review (FDR)
- May 2026: Fabrication, assembly, and testing of FELIX pre-production boards
- Spring 2027: ATLAS Production Readiness Review (PRR)
- Spring 2027: FELIX production begins
- End of 2027: ATLAS production completed